ABSTRACT OF THE DISCLOSURE

A structure of non-volatile memory contains a substrate. A plurality of bit lines are formed in the substrate along a first direction, wherein each of the bit lines also serve as a source/drain (S/D) region. A first dielectric layer is disposed over the substrate. A plurality of selection gate (SG) lines are formed over the first dielectric layer between the bit lines. A plurality of charge-storage structure layer are formed over the substrate between the bit lines and the SG lines. A second dielectric layer is formed over the SG lines and a third dielectric layer is formed over the bit lines. A plurality of word lines are formed over the substrate along a second direction, which is crossing the first direction for the bit lines. Wherein, when a selected one of the SG lines is applied a voltage, another S/D region is created in the substrate under the selected one of the SG lines.